

深圳市金逸晨电子有限公司

ShenZhen GoldenMorning Electronic Co.,Ltd

PRODUCT SPECIFICATION

Model No	E270XN-Y-C24-115
Product Name	2.7 OLED Module
Version	V1.0
Date	2024-11-13

- ☐ Preliminary Specification
☒ Final Specification

PREPARED BY	CHECKED BY	APPROVED BY

Revision History

Version	Date	Page	Revise record	Remarks
1.0	2024.11.13	-	First issued	-

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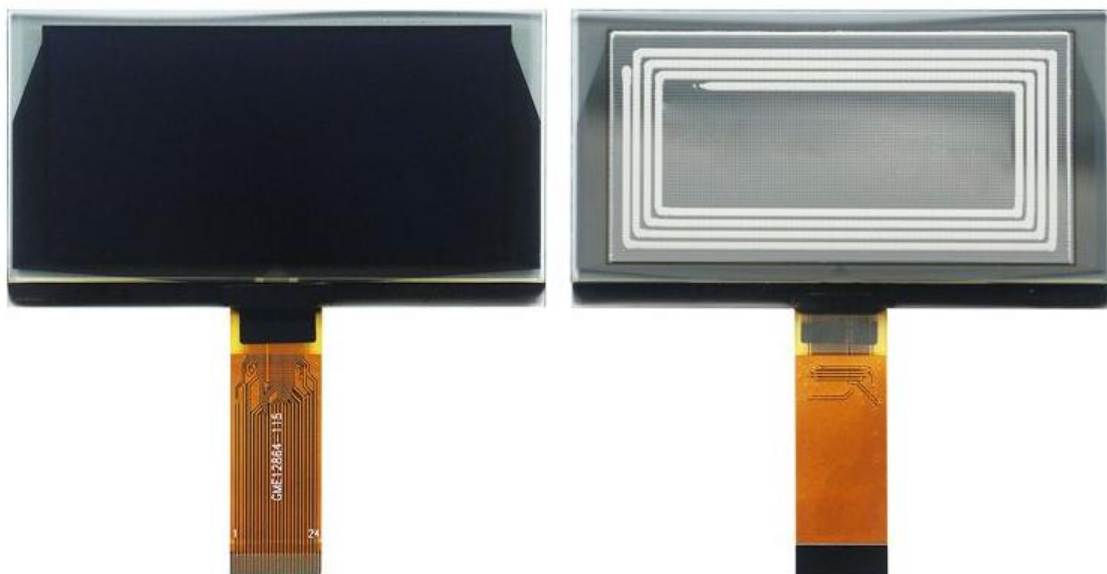
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1. General Parameter

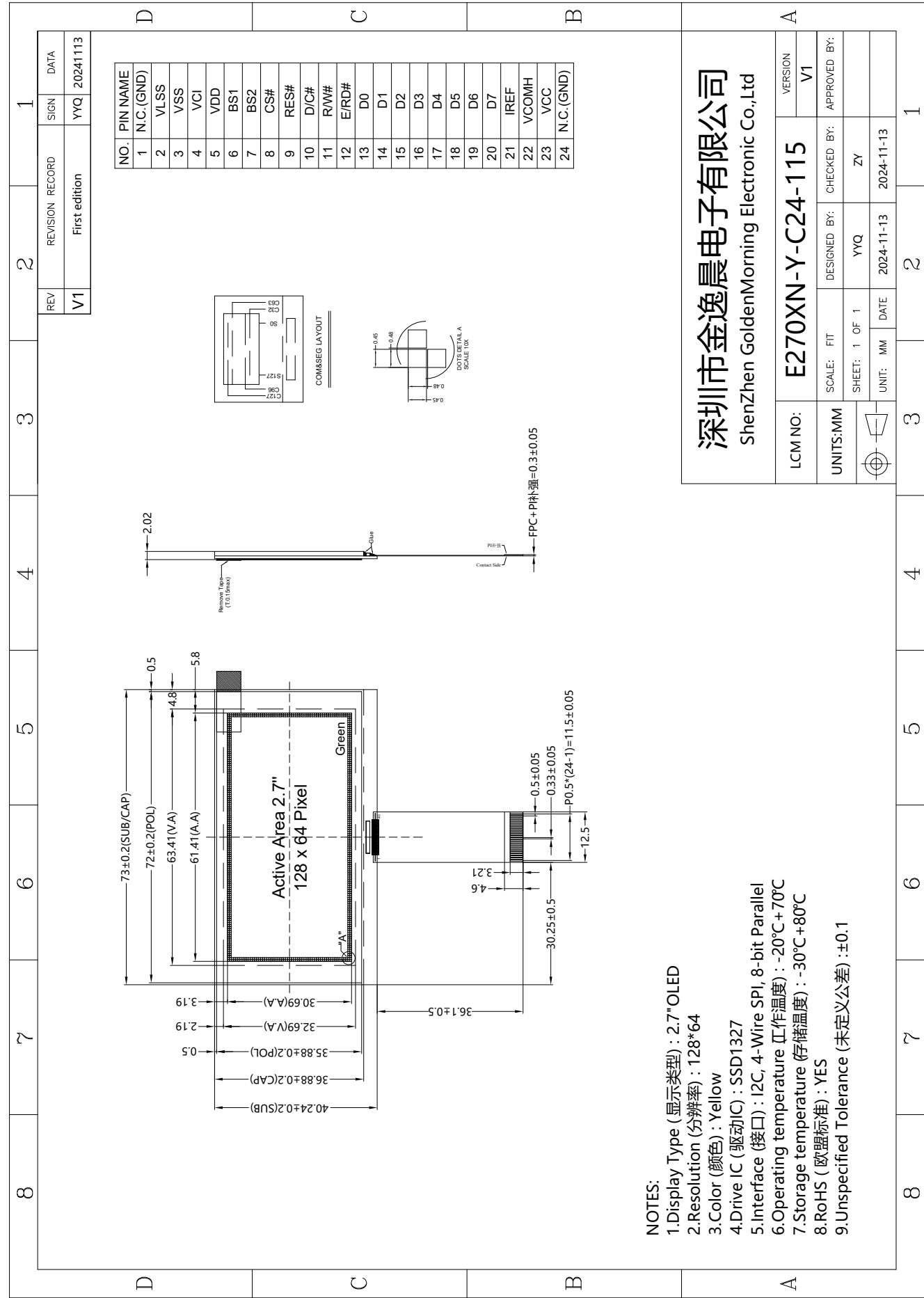
NO.	Features	Details	Unit
1	Display Size(Diagonal)	2.7"	Inch
2	LCD type	OLED	-
3	View Direction	ALL	-
4	Drive Duty	1/64	-
5	Resolution	128 x 64	Pixels
6	Module size	73.00(W) x 40.24(H) x 1.27(T)	mm
7	Active Area	61.41(W) x 30.69(H)	mm
8	Pixel Pitch	0.48(W) x 0.48(H)	mm
9	Pixel Size	0.45(W) x 0.45(H)	mm
10	Interface	I ² C, 4-Wire SPI, 8-bit Parallel	-
11	Display Colors	Yellow	-
12	Driver IC	SSD1327	-
13	IC package type	COG	-
14	Operating Temperature	-20℃~70℃	℃
15	Storage Temperature	-30℃~80℃	℃
16	Weight	12.06	g

Note 1 : Please refer to the mechanical drawing.

2. Physical drawing



3. Mechanical Dimension



4. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	VDD	-0.5	+2.75	V
Low Voltage Power Supply	VCI	-0.3	+4.0	
Operating Voltage	VCC	-0.5	19	V
Operating temperature	Top	-20	70	°C
Storage temperature	Tst	-30	80	°C

Note 1 : All the above voltages are on the basis of “VSS = 0V” .

Note 2 : When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according “Optics & Electrical Characteristics” . If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3 : The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4 : 50% Checkerboard.End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5. DC Characteristics

Condition (Unless otherwise specified): Voltage referenced to VSS VDD = 1.65V to 3.5V TA = 25 °C

Symbol I	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V _{CC}	Operating Voltage	-		8	-	18	V
V _{DD}	Logic Supply Voltage	-		1.65	-	2.6	V
V _{CI}	Low voltage power supply, power supply for I/O pins	-		1.65	-	3.5	V
V _{OH}	High Logic Output Level	I _{out} = 100uA		0.9*V _{CI}	-	V _{CI}	V
V _{OL}	Low Logic Output Level	I _{out} = 100uA		0	-	0.1*V _{CI}	V
V _{IH} ⁽¹⁾	High Logic Input Level	-		0.8*V _{CI}	-	V _{CI}	V
V _{IL} ⁽¹⁾	Low Logic Input Level	-		0	-	0.2*V _{CI}	V
I _{SLP_VDD}	V _{DD} Sleep mode Current	V _{CI} = 2.8V, V _{CC} =OFF V _{DD} (external) = 2.5V, Display OFF, No panel attached		-	-	10	uA
I _{SLP_VCI}	V _{CI} Sleep mode Current	V _{CI} = 2.8V, V _{CC} =OFF Display OFF, No panel attached	External V _{DD} = 2.5V	-	-	10	uA
			Enable Internal V _{DD} during Sleep mode	-	-	40	uA
			Disable Internal V _{DD} during Sleep mode (Deep Sleep mode)	-	-	10	uA
I _{SLP_VCC}	V _{CC} Sleep mode Current	V _{CI} = 2.8V, V _{CC} = 8~18V V _{DD} (external) = 2.5V, Display OFF, No panel attached		-	-	10	uA
I _{DD}	V _{DD} Supply Current	V _{CI} = 3.5V, V _{CC} = 18V, External V _{DD} = 2.5V, Display ON, No panel attached, contrast = FF		-	22	-	uA
I _{CI}	V _{CI} Supply Current	V _{CI} = 3.5V, V _{CC} = 18V, Display ON, No panel attached, contrast = FF	External V _{DD} = 2.5V	-	35	50	uA
			Internal V _{DD} = 2.5V	-	95	120	uA
I _{CC}	V _{CC} Supply Current	V _{CI} = 3.5V, V _{CC} = 18V, Display ON, No panel attached, contrast = FF	External V _{DD} = 2.5V	-	600	750	uA
			Internal V _{DD} = 2.5V	-	600	750	uA
I _{SEG}	Segment Output Current Setting V _{CC} =18V, I _{REF} =10uA	Contrast = FF		-	300	370	uA
		Contrast = AF		-	206	-	uA
		Contrast = 7F		-	150	-	uA
		Contrast = 3F		-	75	-	uA
		Contrast = 1F		-	37.5	-	uA
Dev	Segment output current uniformity	Dev = (I _{SEG} – I _{MID}) / I _{MID} I _{MID} = (I _{MAX} + I _{MIN}) / 2 I _{SEG} = Segment current at contrast FF		-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])		-2	-	2	%

Remarks: (1) Charge pump related pins include: VBAT, C1P, C1N, C2P, C2N, VLSS

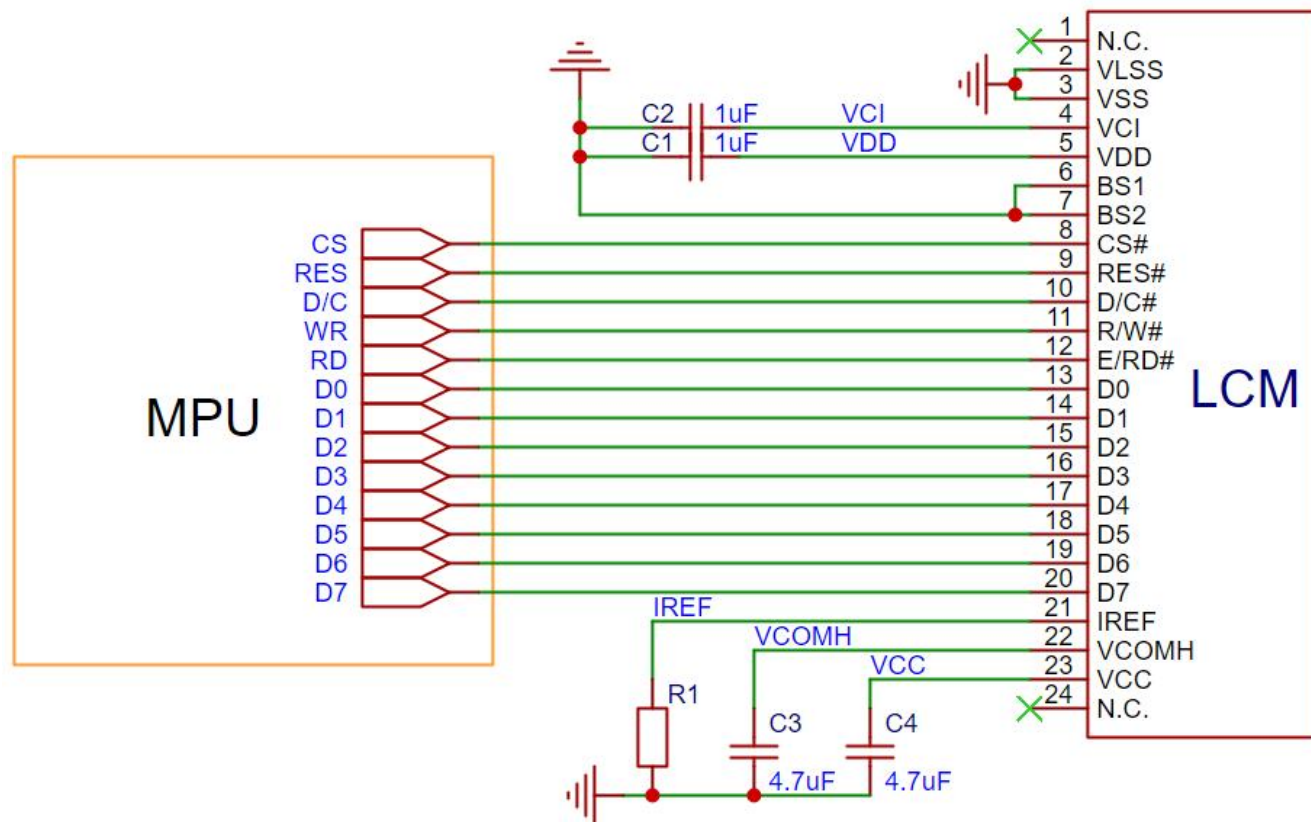
6. Pins Definitions.

Pin.No	Symbol	Description			
1	N.C.	No connect.			
2	VLSS	Analog system ground pin. It must be connected to external ground.			
3	VSS	Ground pin. It must be connected to external ground.			
4	VCI	Low voltage power supply and power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source. VCI must always set to be equivalent to or higher than VDD.			
5	VDD	Power supply pin for core logic operation			
6	BS1	Communicating Protocol Select	Name	8-bit 8080	I ² C
			BS1	1	1
7	BS2		BS2	1	0
				0	0
8	CS#	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).			
9	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to VDD) during normal operation.			
10	D/C#	This is the Data/Command control pad that determines whether the data bits are data or a command. In I ² C interface, this pad serves as SA0 to distinguish the different address of OLED driver.			
11	R/W#	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I ² C interface is selected, this pin must be connected to VSS			
12	E/RD#	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I ² C interface is selected, this pin must be connected to VSS			
13-20	D0-D7	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I ² C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL			
21	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS to maintain the current around 10uA			
22	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS. No external power supply is allowed to connect to this pin.			
23	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.			
24	N.C.	No connect.			

Note 1 : See the IC Specification manual for details.

7. Schematic Diagram.

MCU 8080 8位 参考原理图



Voltage at IREF $\approx$ VCC - 3V.

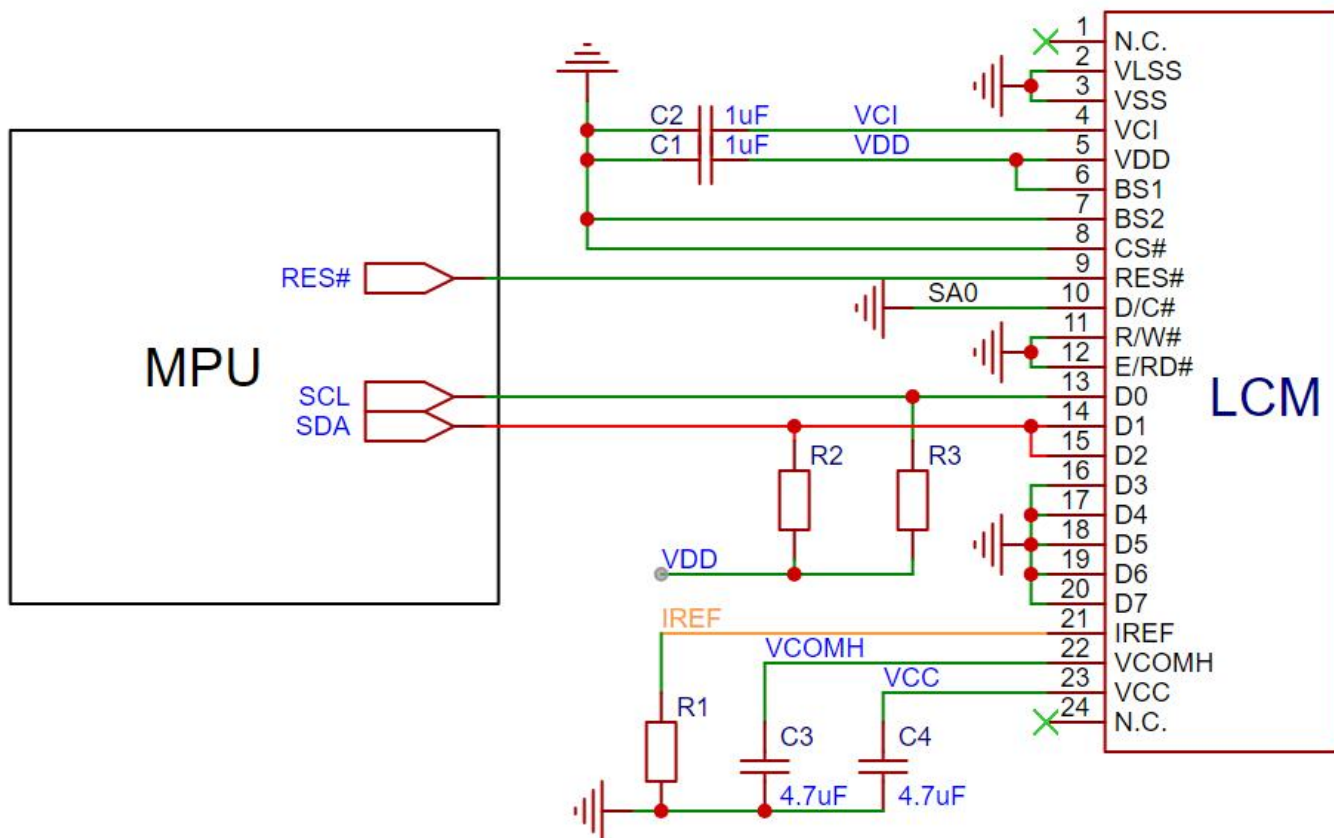
For VCC = 15V, IREF = 10uA:

$$R1 = (\text{Voltage at IREF} - VSS) / IREF$$

$$\approx (15 - 3)V / 10\mu A = 1.2M\Omega$$

$$\begin{aligned} R1 &= (\text{Voltage at IREF} - VSS) / IREF \\ &\approx (15 - 3)V / 10\mu A = 1.2M\Omega \end{aligned}$$

I2C 参考原理图



Voltage at IREF $\approx$ VCC - 3V.

For VCC = 15V, IREF = 10uA:

$R1 = (\text{Voltage at IREF} - VSS) / IREF$

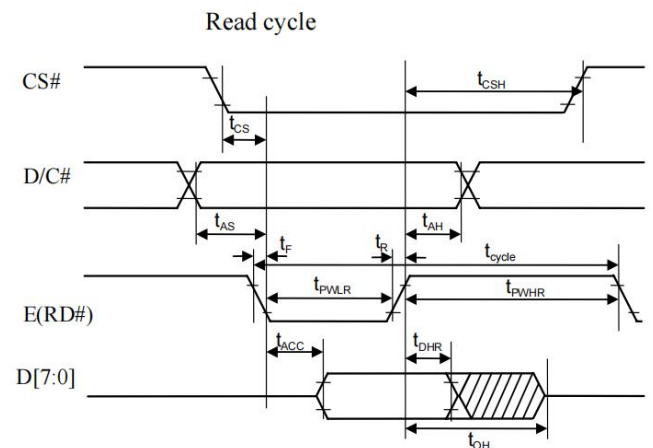
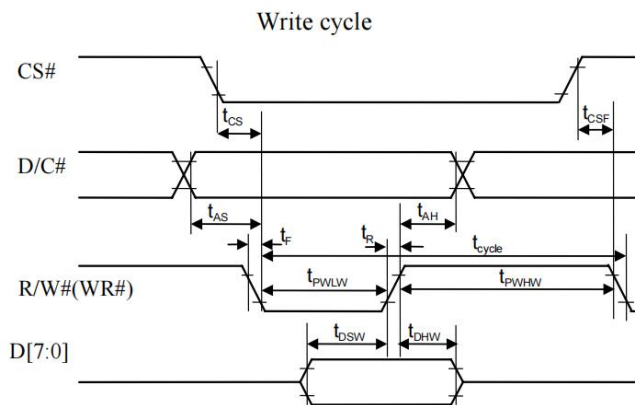
$\approx (15 - 3)V / 10\mu A = 1.2M\Omega$

8. Timing Characteristics.

8080-Series MCU Parallel Interface Timing Characteristics

(VDD - VSS = 1.65V~3.5V, TA = 25°C)

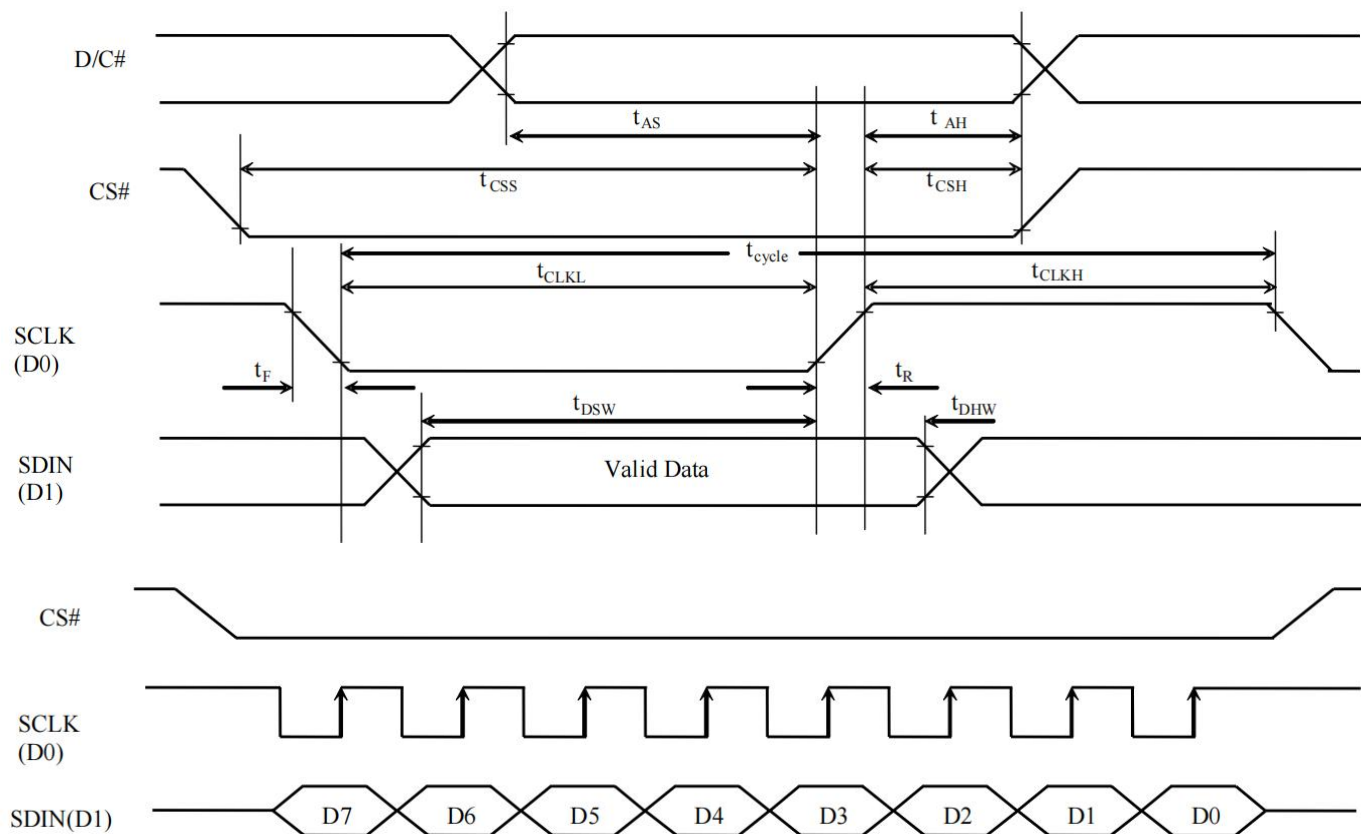
Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	-	ns
t _{AS}	Address Setup Time	10	-	-	ns
t _{AH}	Address Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	40	-	-	ns
t _{DHW}	Write Data Hold Time	7	-	-	ns
t _{DHR}	Read Data Hold Time	20	-	-	ns
t _{OH}	Output Disable Time	-	-	70	ns
t _{ACC}	Access Time	-	-	140	ns
t _{PWLR}	Read Low Time	150	-	-	ns
t _{PWLW}	Write Low Time	60	-	-	ns
t _{PWHR}	Read High Time	60	-	-	ns
t _{PWHW}	Write High Time	60	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns
t _{CS}	Chip select setup time	0	-	-	ns
t _{CSH}	Chip select hold time to read signal	0	-	-	ns
t _{CSF}	Chip select hold time	20	-	-	ns



Serial Interface Timing Characteristics (4-wire SPI)

(VDD - VSS = 1.65V~3.5V, TA = 25°C)

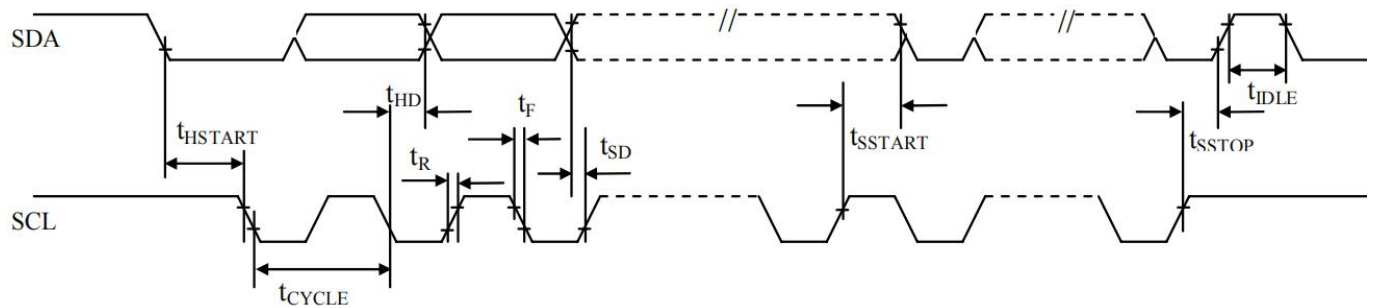
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_{R}	Rise Time	-	-	15	ns
t_{F}	Fall Time	-	-	15	ns



I2C Interface Timing Characteristics

(VDD - VSS = 1.65V~3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA _{OUT} " pin)	0	-	-	ns
	Data Hold Time (for "SDA _{IN} " pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_{R}	Rise Time for data and clock pin	-	-	300	ns
t_{F}	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



9. Optical Characteristics.

All data in below based the condition (Ta = 22±3℃,60±10%RH).

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	60	75	-	cd /m ²	All pixels ON
Power Consumption		P	-	250	310	mW	30% pixels ON
Frame Frequency		Fr	-	100	-	Hz	-
Color Coordinate	Yellow	CIE x	0.42	0.46	0.50	CIE1931	Darkroom
		CIE y	0.49	0.53	0.57		
Response Time	Rise	Tr	-	10	-	us	-
	Decay	Td	-	10	-	us	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle		△θ	160	-	-	Degree	-
Operating Life Time*		Top	50000	-	-	Hours	L=75cd/m2

Note:

(1) 75cd/m² is based on VDD=3.0V,VCC=15V,Contrast command setting : 0XDF. 75cd/m²

(2) Contrast ratio is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

(3) Life Time is defined when the Luminance has decayed to less than 50% of the initial Luminance specification.

(Odd and even chess board alternately displayed). (The initial value should be closed to the typical value after adjusting.)

10. Reliability

10.1. MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal.

10.2. Test Condition

No	Item	Condition	Criteria
1	High Temperature Operating	70℃*24Hrs	1. No Defect Of Operational Function In Room Temperature Are Allowable. 2. IDD of LCM in Pre-and Post-Test Should Follow Specification.
2	Low Temperature Operating	-20℃*24Hrs	
3	High Humidity Storage	50℃*90%RH*24Hrs	
4	High Temperature Storage	80℃*24Hrs	
5	Low Temperature Storage	-30℃*24Hrs	
6	Thermal Cycling Test Storage	-	
7	Packing vibration	-	
8	Electrical Static Discharge	-	
		-	
9	Drop Test (Packaged)	-	

Note 1 : The test samples should be applied to only one test item.

Note 2 : Sample size for each test item is 2pcs.

Note 3 : No defective function allowable.

11. Precautions

11.1. Storage Conditions

- 11.1.1. Store the panel or module in a dark place where the temperature is $23\pm5^{\circ}\text{C}$ and the humidity is below $45\pm 20\%\text{RH}$.
- 11.1.2. Store in anti-static electricity container.
- 11.1.3. Store in clean environment, free from dust, active gas, and solvent.
- 11.1.4. Do not place the module near organics solvents or corrosive gases.
- 11.1.5. Do not crush, shake, or jolt the module.
- 11.1.6. Strong light exposure causes degradation of polarizer and color filter.

11.2. Handling Precautions

- 11.2.1. Avoid static electricity, which can damage the CMOS LSI.
- 11.2.2. The polarizing plate of the display is very fragile, please handle it very carefully.
- 11.2.3. Do not give external shock.
- 11.2.4. Do not apply excessive force on the surface.
- 11.2.5. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.
- 11.2.6. Reverse and use within ratings in order to keep performance and prevent damage
- 11.2.7. Do not remove the panel or frame from the module.
- 11.2.8. Except for soldering the interface, do not make any alterations or modifications with a soldering iron; Ensure welding temperature at 320°C to 350°C , the welding time control within the 10 s, welding note don't stay too long in the same place to avoid scald FPC.

11.3. Limited Warranty

- 11.3.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss. (我们的保证责任仅限于修理和/或更换。我们将不负任何相应的损失。)
- 11.3.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used. (如果可能，我们建议客户在 6 个月内用完所有模块。如果模块存放时间超过 12 个月，我们建议在使用模块前重新检查。)
- 11.3.3. The warranty period is twelve months from the date of delivery. Buyer shall complete the assembly of all processes within twelve months of validity. During the warranty period, if the product quality problems, our company will be responsible for repair and replacement. All products must be stored and handled in accordance with regulations. Under warranty. When the goods do not comply with the above terms, we do not provide warranty services. (保修期为交货之日起十二个月。买方应在 12 个月内完成所有流程的组装。在保修期内，如果产品出现质量问题，我公司将负责维修和更换。所有产品必须按照规定储存和处理。在保修期内。当货物不符合上述条款时，我们不提供保修服务。)