

DATA SHEET

LCD MODULE

GME64128-02

SH1107-64128-1.3-4pin模块GND开头

Product specification

Version: 1

9/Apr/2022

GENERAL SPECIFICATION

MODULE NO. :

GME64128-02

CUSTOMER P/N:

VERSION NO.	CHANGE DESCRIPTION	DATE
1	ORIGINAL VERSION	2022/04/09

PREPARED BY: _____

DATE: 2022/04/09

APPROVED BY: _____

DATE: 2022/04/09

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1. FUNCTIONS & FEATURES

- LCD TYPE:

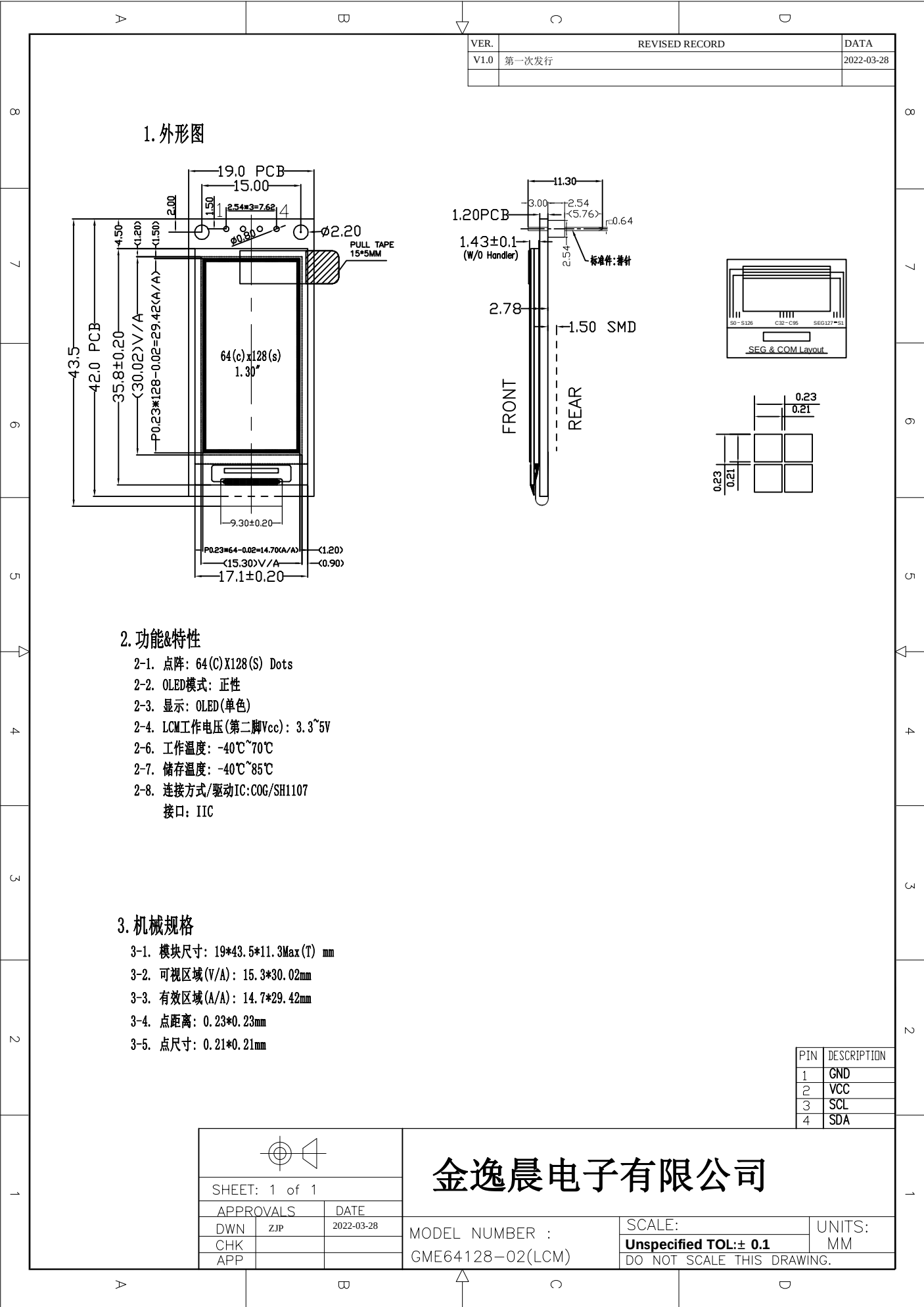
MODULE MODEL	LCD TYPE	REMARK
2864KLBLG03	1.30" OLED Passive Matrix White	

- Driving Scheme : 1/64 Duty,
- Viewing direction : ALL
- Drive IC : SH1107
- Operating voltage (VDD) : 3.3 V
- Vpp : 12.0V
- Interface :IIC
- RoHS Compliant

2. MECHANICAL SPECIFICATIONS

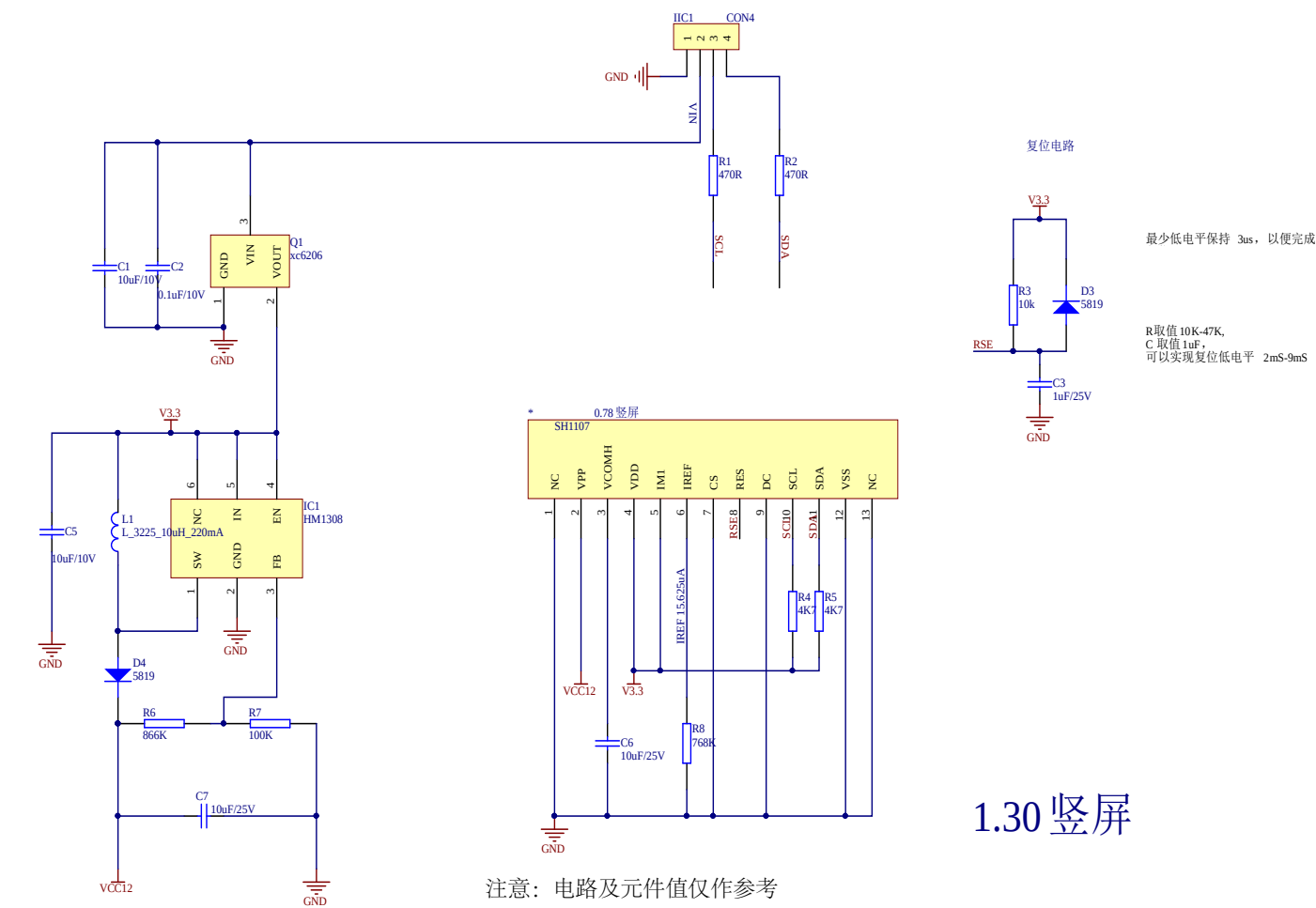
- Module Size : 42x19x11.30(max)mm
- Viewing Area : 30.02(L) x 15.30 (W) mm
- Active Area : 29.42 (L) x 14.70 (W) mm
- Dot Pitch : 0.23 (W) x 0.23 (H) mm
- Dot Size : 0.21(W) x 0.21(H) mm

3. EXTERNAL DIMENSIONS (单位: mm)



4. SCH DIAGRAM

原理图：



5. PIN ASSIGNMENT

Pin no.	Symbol	Function
1	GND	地
2	Vcc	模块供电电源正
3	SCL	时钟
4	SDA	数据

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V_{PP}	7	16.5	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (150 cd/m ²)		10,000	-	hour	4

Note 1: All the above voltages are on the basis of " $V_{SS} = 0V$ ".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

7. ELECTRICAL CHARACTERISTICS

7.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{PP} Supplied Externally)	L_{br}	Note 4	120	160	-	cd/m ²
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at $V_{DD} = 2.8V$, $V_{PP} = 9V$.

Software configuration follows Section 4.5 Initialization.

7.2. DC CHARACTERISTICS

DC Characteristics (VSS = 0V, VDD = 1.65 - 3.5V AVDD=2.4-3.5V, TA =+25°C, unless otherwise specified)

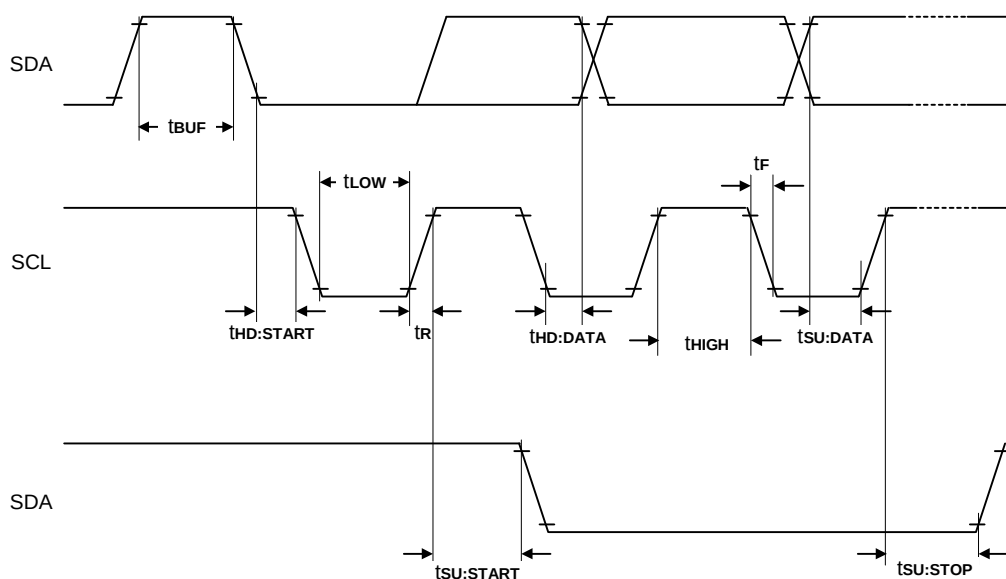
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage	1.65	-	3.5	V	
AVDD	DC-DC voltage	2.4	3.0	3.5	V	
VPP	OLED Operating voltage	7	15	16.5	V	
VBREF	Internal voltage reference	1.15	1.20	1.25	V	
IDD1	Dynamic current consumption 1(in VDD)	-	110	160	μA	VDD = 3V, AVDD=3V, IREF = -15.625μA, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached.
IDD2	Dynamic current consumption 2 (in AVDD)	-	190	285	μA	VDD=3V, AVDD=3V, IREF = -15.625μA, Contrast α = 256, Bulid-in DC-DC ON, VPP=15V, Display ON, display data = All ON, No panel attached.
Ipp	OLED dynamic current consumption	-	1	1.27	mA	VDD = 3V, AVDD = 3V, VPP = 15V, IREF = -15.625μA, Contrast α = 256, Display ON, Display data = All ON, No panel attached
ISP	Sleep mode current consumption in VDD & AVDD	-	0.01	5	μA	During sleep, TA = +25°C, VDD = 3V, AVDD=3V
	Sleep mode current consumption in VPP	-	0.01	5	μA	During sleep, TA = +25°C, VPP = 15V (External)
ISEG	Segment output current	-	-500	-	μA	VDD = 3V, VPP = 15V, IREF = -15.625μA, RLOAD = 20kΩ, Display ON. Contrast α = 256.
		-	-343.75	-	μA	VDD = 3V, VPP = 15V, IREF = -15.625μA, RLOAD = 20kΩ, Display ON. Contrast α = 176.
		-	-187.5	-	μA	VDD = 3V, VPP = 15V, IREF = -15.625μA, RLOAD = 20kΩ, Display ON. Contrast α = 96.
		-	-31.25	-	μA	VDD = 3V, VPP = 15V, IREF = -15.625μA, RLOAD = 20kΩ, Display ON. Contrast α = 16
ΔISEG1	Segment output current uniformity	-	-	±3	%	$\Delta ISEG1 = (ISEG - IMID)/IMID \times 100\%$ $IMID = (IMAX + IMIN)/2$ ISEG [0:131] at contrast α = 256.
ΔISEG2	Adjacent segment output current uniformity	-	-	±2	%	$\Delta ISEG2 = (ISEG[N] - ISEG[N+1])/(ISEG[N] + ISEG[N+1]) \times 100\%$ ISEG [0:131] at contrast α = 256.

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VIHC	High-level input voltage	0.8 X VDD	-	VDD	V	A0, D0 - D7, RD (E), WR (R/W), CS, CLS, CL, IM0~2 and RES.
VILC	Low-level input voltage	VSS	-	0.2 X VDD	V	
VOHC	High-level output voltage	0.8 X VDD	-	VDD	V	IOH = -0.5mA (D0 - D7, and CL).
VOLC	Low -level output voltage	VSS	-	0.2 X VDD	V	IOL = 0.5mA (D0, D2 - D7, and CL)
VOLCS	SDA low -level output voltage	VSS	-	0.2 X VDD	V	VDD<2V IOL=2mA (SDA)
				0.4		VDD>2V IOL=3mA (SDA)
ILI	Input leakage current	-1.0	-	1.0	μA	VIN = VDD or VSS (A0, RD (E), WR (R/W), CS, CLS, IM0~2 and RES).
IHz	Hz leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
fOSC	Oscillation frequency	-	720	-	kHz	TA = +25°C.VDD=3V
fFRM	Frame frequency for 128 Commons	-	104	-	Hz	When fosc = 720kHz, Divide ratio = 1, common width = 54 DCLKs.
RON1	Common switch resistance	-	15	-	Ω	Vpp=15V,Vcom=Vss+0.4V
RON2	Common switch resistance	-	500	-	Ω	Vpp=15V,VCOM=0.770×Vpp-0.4V

7.3.AC CHARACTERISTICS

Version: 1

I²C interface characteristics(V_{DD} = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f _{SCL}	SCL clock frequency	DC	-	400	kHz	
T _{LOW}	SCL clock Low pulse width	1.3	-	-	μs	
T _{HIGH}	SCL clock H pulse width	0.6	-	-	μs	
T _{SU:DATA}	data setup time	100	-	-	ns	
T _{HD:DATA}	data hold time	0	-	0.9	μs	
T _R	SCL, SDA rise time	20+0.1Cb	-	300	ns	
T _F	SCL, SDA fall time	20+0.1Cb	-	300	ns	
C _b	Capacity load on each bus line	-	-	400	pF	
T _{SU:START}	Setup time for re-START	0.6	-	-	μs	
T _{HD:START}	START Hold time	0.6	-	-	μs	
T _{SU:STOP}	Setup time for STOP	0.6	-	-	μs	
T _{BUF}	Bus free times between STOP and START condition	1.3	-	-	μs	

8. COMMANDS

Command Table

Command	Code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2.Set Column Address 4 higher bits	0	1	0	0	0	0	1	0	Higher column address			Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3.Set memory addressing mode	0	1	0	0	0	1	0	0	0	0	D	D = 1, Vertical Addressing Mode D = 0, Page Addressing Mode (POR=20H)
4. The Contrast Control Mode Set Contrast Data Register Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
	0	1	0	Contrast Data								
5. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The down (0) or up (1) rotation. (POR = A0H)
6. Set Multiplex Ration	0	1	0	1	0	1	0	1	0	0	0	This command switches multiplex mode to any multiplex ratio from 1 to 128. (POR = 7FH)
	0	1	0	-	Multiplex Ratio							
7. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
8. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
9. Set display offset	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command that specifies the mapping of display start line to one of COM0 -127. (POR = 00H)
	0	1	0	-	COMx							
10. DC-DC Control Mode Set DC-DC Setting Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 81H)
	0	1	0	1	0	0	0	F2	F1	F0	D	

Command Table (Continued)

Command	Code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
11. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
12. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
13 Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
14. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
15. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
16. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM = (β ₁ X VREF)								
17. Set Display Start Line	0	1	0	1	1	0	1	1	1	0	0	Specify RAM display line for COM0.
	0	1	0	-	Start line							
18. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
19. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
20. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
21 Write Display Data	1	1	0	Write RAM data								
22 Read ID	0	0	1	BUSY	ON/ OFF	ID						
23. Read Display Data	1	0	1	Read RAM data								

Note: Do not use any other command, or the system malfunction may result.

9. FUNCTIONAL SPECIFICATION

9.1 Commands

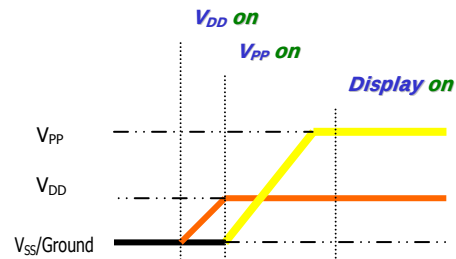
Refer to the Technical Manual for the SH1107

9.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

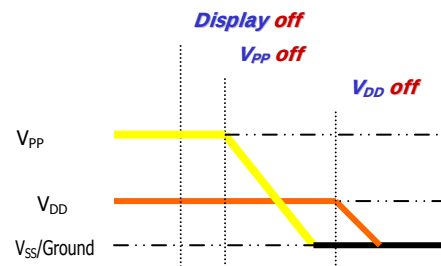
9.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VPP
6. Delay 100ms
(When VPP is stable)
7. Send Display on command



9.2.2 Power down Sequence:

1. Send Display off command
2. Power down VPP
3. Delay 100ms
(When VPP is reach 0 and panel is completely discharges)
4. Power down VDD



Note 9:

- 1) Since an ESD protection circuit is connected between VDD and VBPPB inside the driver IC, VPP becomes lower than VDD whenever VBDDDB is ON and VPP is OFF.
- 2) VPPB should be kept float (disable) when it is OFF.
- 3) Power Pins (VDD, VPP) can never be pulled to ground under any circumstance.
- 4) VBDDDB should not be power down before VPP power down.

9.3 Reset Circuit

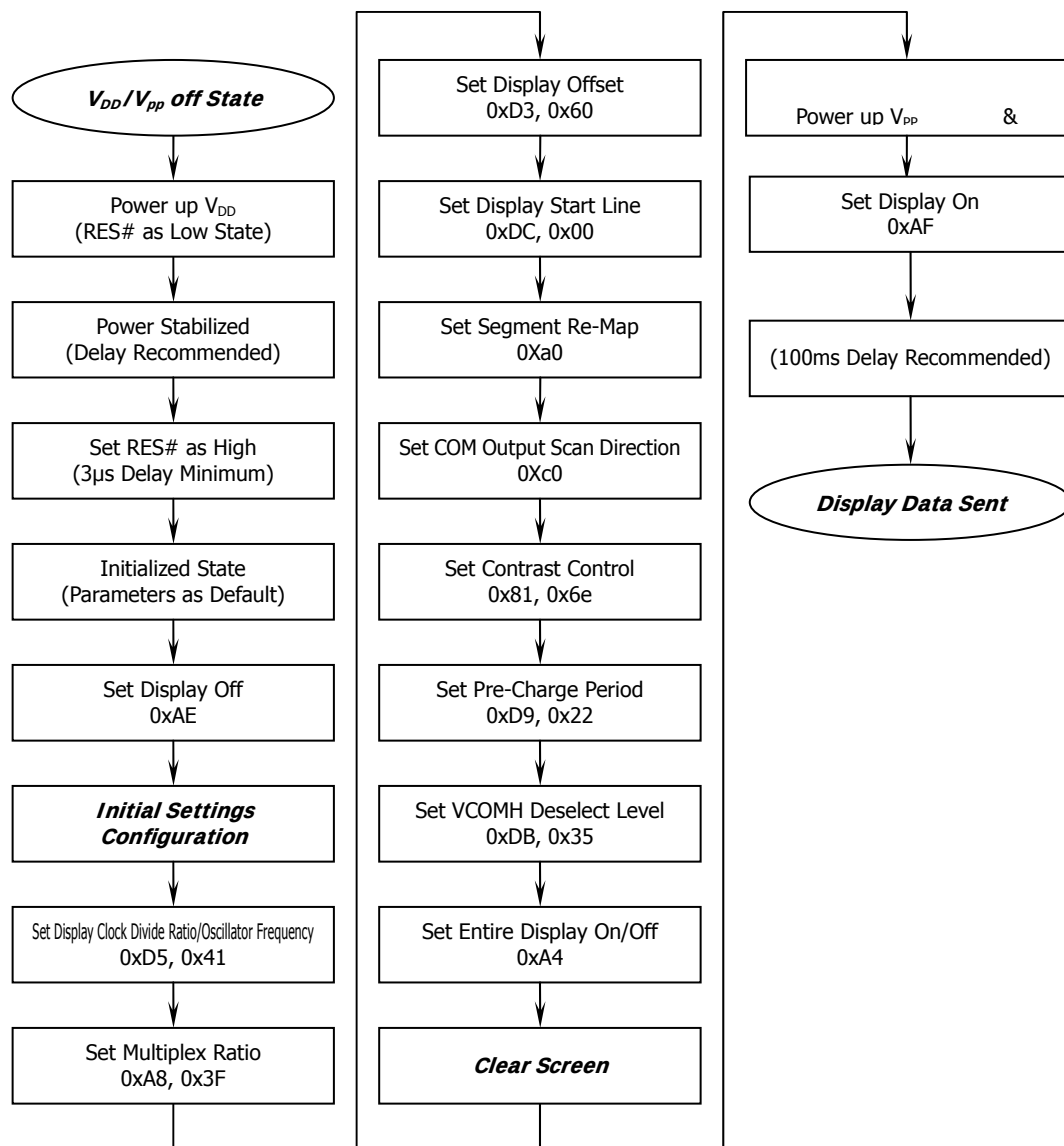
When RESB input is low, the chip is initialized with the following status:

1. Display is OFF. Common and Segment are in high impedance state.
2. 128~128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

9.4 Actual Application Example

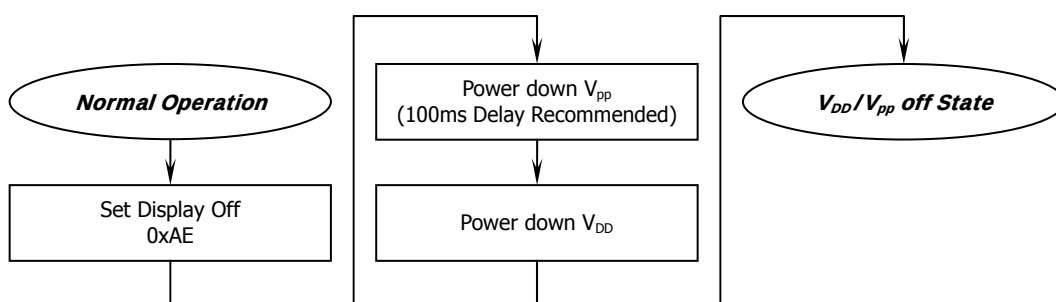
Command usage and explanation of an actual example

9.4.1 V_{pp} Supplied Externally

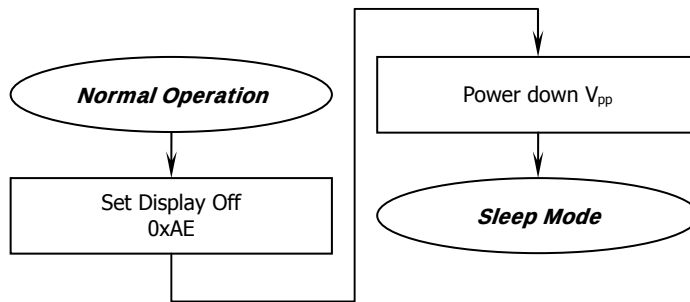


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

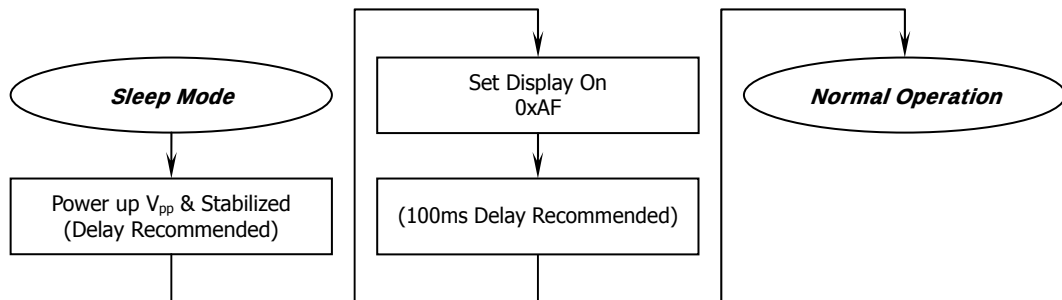
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



10. MODULE ACCEPT QUALITY LEVEL (AQL)

10.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

10.2 Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level II

11. RELIABILITY TEST.**11.1 Contents of Reliability Tests**

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

11.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

12. QUALITY DESCRIPTION & APPLICATION NOTE

Please refer to "General Inspection Criteria" document.